Green Hills Debug Probes Release Notes

Green Hills Software
30 West Sola Street
Santa Barbara, California 93101
USA
Tel: 805-965-6044
Fax: 805-965-6343
www.ghs.com

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Preface

Contents

Thank you for choosing a Green Hills debug probe. These release notes cover what is new in this probe firmware release, what has changed, and other release-specific information that is not available in the standard documentation.

For installation information and instructions that explain how to configure your probe for your target, see the *Getting Started* book for your probe.

For reference information, see the *Green Hills Debug Probes User's Guide*.

Host System Requirements

Green Hills debug probe software runs on the same operating systems as MULTI. If your installation disc contains only debug probe software, you can use it to upgrade MULTI 5, or 6. If your disc contains MULTI, the Green Hills Compiler, and Probe software, you can use it to upgrade MULTI 6.

If you upgrade MULTI 4, the probe firmware and support software version 4.4.2 will be installed, which is the newest version to support MULTI 4.

The installation requires 40 MB of disk space.

Chapter 1

Version 5.2.2 Release Notes

Contents

This document covers changes to the Green Hills Probe firmware that were added for version 5.2.

New Features

New Supported Targets

Support for the following targets was added in version 5.2.2:

- Avago AXX55xx (`axx5500`)
- Freescale MPC577xK (`ppc5775K`)
- Freescale QorIQ T4160 (`ppcT4160`)
- Freescale QorIQ T4240 (`ppcT4240`)

Additional New Project Wizard Support

New Project Wizard support for the following boards was added in version 5.2.2:

- Freescale MPC5775K Demo Board
- Freescale T4240DS

Support for these boards will be installed into Compiler 2012.5 or newer.

New Trace Support

The SuperTrace Probe v3 now supports debugging and tracing the following targets:

- Freescale Qorivva 57xx targets, over the high-speed serial trace (HSST) Aurora interface.

New Flash Support

The following flash chips are now supported:

- MPC57xx and SPC57x processors – for more information, see “Programming the UTest Block on MPC57xx and SPC57x” in Appendix D, “Troubleshooting and Usage Notes” in *Green Hills Debug Probes User's Guide*.

New Support for Synchronous Multi-Core Systems

The probe now supports locking cores in a multi-core system, so that all cores in the system always resume and halt at the same time. This feature also enables software breakpoints to be set on all cores at the same time. For more information, see **Halt cores synchronously** in “Green Hills Debug Probe (mpserv) Advanced Settings” in Chapter 3, “Probe Connection Reference” in *Green Hills Debug Probes User's Guide*. This feature is only supported on ARM Cortex-A and POWER e500mc, e5500, and e6500 targets at this time, and requires MULTI 7 or later.

New Feature Support for Cortex-A15

The following features are now supported on the Cortex-A15:

- L1 and L2 cache visualization
- TLB visualization
- Trace Support

TMC-ETB Support Added

This release adds support for ARM's Trace Memory Controller when configured as an Embedded Trace Buffer (TMC-ETB). This feature allows targets containing a TMC-ETB to be tracked with a Green Hills Probe as well as a SuperTrace Probe.

Support for Heterogeneous Multi-Core CoreSight Systems

The Green Hills Probe now supports debugging systems that contain multiple CPU cores of different types behind a single CoreSight DAP. See “Specifying CoreSight Targets” in Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide* for more information.

Probe Configuration Files Automatically Added to Projects and Loaded at Connection to MULTI

When creating a project with the New Project Wizard, if a probe configuration file exists for the target you select, that file will be copied into the new project and will be added to the **Probe Config** tab of the Connection Editor. When you connect to MULTI, the settings in that file will be written to the probe, and will override any current settings on the probe. If you want your probe settings to remain unchanged, you can remove the file from the Connection Editor, and no settings will be written to the probe. If you would like to modify the settings that are written to the probe, you may save your probe's current configuration using the following command:

```
mpadmin -cfgsave probe filename
```

For more information, see "Loading and Saving Configuration Files" in Chapter 1, "Administering Your Probe" in *Green Hills Debug Probes User's Guide* and "Green Hills Debug Probe (mpserv) Probe Config Settings" in Chapter 3, "Probe Connection Reference" in *Green Hills Debug Probes User's Guide*.

IEEE 1149.7 cJTAG Support for Freescale Targets

The Green Hills Probe now supports reduced-pin IEEE 1149.7 debug modes on Freescale MPC57xx and Kinetis targets. For more information, see the documentation about the **debug_type** option in "Selecting the Target Communication Protocol" in Chapter 4, "Probe Option Reference" in *Green Hills Debug Probes User's Guide*.

For IEEE 1149.7 support for other targets, please contact Green Hills Support.

Support Added for MPC5744P Cut 2

The probe firmware, register definitions, and New Project Wizard entry all now support the Freescale MPC5744P cut 2 silicon.

Improved Support for Freescale Vybrid

The `vybrid` target setting now also debugs the Vybrid's Cortex-M4 core (in addition to the Cortex-A5). Vybrid CPUs that are configured with Cortex-M4 as the primary core can be debugged with the `vybrid.m4pri` target setting.

New Probe Configuration Options

GTL-capable adapters (used for x86 targets) now present a **use_gtl** option which can be used to control the use of the GTL drivers. For more information, see **use_gtl** in "x86" in Chapter 4, "Probe Option Reference" in *Green Hills Debug Probes User's Guide*.

The probe now allows users to configure how a soft reset is performed on Cortex-A8 targets via the new **rst_dpll3** configuration option. For more information, see "ARM" in Chapter 4, "Probe Option Reference" in *Green Hills Debug Probes User's Guide*.

Changes in Behavior

use_swd Configuration Option Removed

The **use_swd** configuration option has been removed. The functionality formerly provided by **use_swd** is now available with the **debug_type** option. For more information, see "Selecting the Target Communication Protocol" in Chapter 4, "Probe Option Reference" in *Green Hills Debug Probes User's Guide*

New Syntax for Specifying CoreSight Targets

CoreSight targets are specified using the target setting `csdap()` which describes the set of CoreSight cores and peripherals. Note that the earlier target settings used to specify CoreSight targets will remain in the firmware but are considered deprecated.

When using the new `csdap()` syntax, the probe does not scan the ROM Table to set `cortex_addr`, `etm_addr`, `ptm_addr`, `tpiu_addr` or `tpiu_type`. In addition, the probe no longer automatically detects the index of the AHB-AP, AXI-AP or

APB-AP, but provides new options to specify the index. These options must be correctly set for proper debug operation. In most cases, the **detect** command is able to detect the correct values. For more information, see "Specifying CoreSight Targets" in Chapter 4, "Probe Option Reference" in *Green Hills Debug Probes User's Guide*.

detect Command Changes

The **detect** command now detects several options in addition to `target` and `endianness`. Furthermore, for a target that has a CoreSight DAP, the detected values for `target` use the new syntax described in "Specifying CoreSight Targets" in Chapter 4, "Probe Option Reference" in *Green Hills Debug Probes User's Guide*.

Big Endian Cortex-M Targets Now Supported

Cortex-M targets are now supported in Big Endian data mode. The **inst_endianness** option may be used to select the instruction endianness when in Big Endian data mode.

Removed Features

MPC5746M and MPC5777M e200z0 Core No Longer Available

Debug access to the e200z0 core on MPC5746M and MPC5777M is no longer present in the v5.2 firmware. Contact Green Hills Support if you require debug access to the e200z0 core on these devices.

Chapter 2

Version 5.0.8 Release Notes

Contents

This document covers changes to the Green Hills Probe firmware that were added for version 5.0.

New Features

New Supported Targets

Support for the following targets was added in version 5.0.8:

- Cortex-R5 (`cortexr5`)
- Cortex-A15 (`cortexa15`)
- TI OMAP5432 (`omap5`)

Support for the following targets was added in version 5.0.4:

- Cortex-M0+ (`cortexm0`)
- Cortex-A5 (`cortexa5`)
- Freescale Vybrid (`vybrid`)
- Freescale MPC5602P (`ppc560xP.n1`)
- Freescale MPC5602D (`ppc560xB.n1`)
- Freescale MCF 5301x (`mcf5301x`)
- Freescale QorIQ P2041 (`ppcP2041`)
- Freescale QorIQ P5020 (`ppcP5020`)
- Freescale QorIQ P5040 (`ppcP5040`)
- Freescale MPC5744K (`ppc5744K`)
- Freescale MPC5746R (`ppc5746R`)
- Freescale MPC5748G (`ppc5748G`)
- Freescale MPC5777M (`ppc5777M`)
- Fujitsu FCR4 (`fcr4`)
- MIPS 14K (`mips32_14kc`, `mips32_14kf`)
- MIPS 74K (`mips32_74kc`, `mips32_74kf`)
- MIPS 1004K (`mips32_1004kc`, `mips32_1004kf`)

- ST Micro SPC56AP60 (`spc56AP60`)
- ST Micro SPC570S50 (`spc570S50`)
- ST Micro SPC572L64 (`spc572L64`)
- ST Micro SPC574K72 (`spc574K72`)
- TI AM389x (`am389x`)
- Xilinx Zynq (`cortexa9`)

Additional New Project Wizard Support

New Project Wizard support for the following board was added in version 5.0.8:

- TI OMAP5432 uEVM ES2.0 GP

New Project Wizard support for the following boards was added in version 5.0.4:

- Atmel SAMA5 D3x Evaluation Kit
- Freescale iMX6-based targets:
  - Freescale Armadillo 2
  - Boundary Devices Nitrogen 6X
  - Boundary Devices SabreLite
- Freescale Kinetis K20
- Freescale Kinetis K53
- Freescale Kinetis KL25Z
- Freescale MCF53015EVB
- Freescale MPC5744K Demo Board
- Freescale MPC5746R Demo Board
- Freescale MPC5748G Demo Board
- Freescale MPC5777M Demo Board
- Freescale P2041RDB
- Freescale P5020DS
- Freescale P5040DS
- Freescale PX TWR PXD10

- Freescale PX TWR PXD20
- Freescale PX TWR PXN20
- Freescale PX TWR PXR40
- Freescale PX TWR PXS20
- Freescale PX TWR PXS30
- Freescale TWR-VF65GS10 (Vybrid)
- Fujitsu SK-MB9DF125 (Atlas-L)
- Fujitsu SK-MB9EF120 (Calypso)
- ST SPC56AP60
- ST SPC570S50 EVB
- ST SPC574K72 Demo Board
- ST SPC572L64 EVB
- TI AM335x EVM or BeagleBone
- TI RM42 Hercules Development Kit
- TI RM46 Hercules Development Kit
- TI RM48 Hercules Development Kit
- TI TMS570LS31x Hercules Development Kit
- TI TMS570LS12x Hercules Development Kit
- TI TMS570LS04x Hercules Development Kit
- Xilinx Zynq

Support for these boards will be installed into Compiler 2012.1 or newer.

New Trace Support

The SuperTrace Probe v3 now supports debugging and tracing the following targets:

- ColdFire v2, v3, and v4 targets (requires MULTI 6 or newer)
- ARM Cortex targets with a Program Trace Macrocell (PTM) interface, such as the Cortex-A9 (requires MULTI 6 or newer)
- PowerPC 405

- Freescale QorIQ e500mc and e5500 targets, over the high-speed serial trace (HSST) Aurora interface.
- Serial STPv3 can now collect PTM trace on Cortex-A9 targets via the Serial trace interface.

New Support for Target Trace Buffers

This release adds support for embedded trace buffers (ETB) on Cortex-R and Cortex-A targets for which trace is already supported. This feature allows these targets to be traced with a Green Hills Probe, as well as with a SuperTrace Probe v3. See “Supported Devices” in Appendix E, “Supported Devices and Adapter Types” in *Green Hills Debug Probes User's Guide* for information about for more information about which targets have a supported ETB.

AXI-AP Support Added

The probe now supports the AXI-AP bus, which is present on certain Cortex devices. For more information, see “Target-Specific Special Registers” in Chapter 5, “Probe Command Reference” in *Green Hills Debug Probes User's Guide*.

New TraceEverywhere Parallel Trace Interface

This release includes support for a new TraceEverywhere trace pod that supports all existing TE5 adapters and allows the SuperTrace Probe v3 to connect to a much wider set of targets.

Support Through the High-Speed Serial Trace (HSST) Aurora Interface

As of this release, the SuperTrace Probe v3 supports debugging and tracing using the high speed serial trace Aurora interface. This firmware includes support for ARM CoreSight trace on Cortex-R4 and PowerPC Nexus, in both 1 lane and 2 lane configurations.

Probe Run Mode Support

This release adds support for Probe Run Mode for INTEGRITY, allowing targets with live memory access, such as PowerPC and ARM Cortex, to be debugged with a run-mode connection via the JTAG interface without the use of a dedicated serial or Ethernet port on the target, and without halting the target via JTAG. For more information, see “Probe Run Mode” in Chapter 3, “Probe Connection Reference” in *Green Hills Debug Probes User's Guide*.

Faster Power Architecture Trace Decoders

This release includes a new PowerPC 440 and Nexus e200 trace decoders that increase decompression performance and improve reliability. These decoders require MULTI 6 or newer.

New Options for Fujitsu FCR4 Processors

New options have been added to configure the base addresses and size of tightly-coupled memory (TCM). For more information, see “ARM” in Chapter 4, “Probe Option Reference” in *Green Hills Debug Probes User's Guide*.

Programming Spansion SPI Flash Memory Chips from Renesas RZ/A1

Support has been added for programming Spansion SPI flash memory chips from the Renesas RZ/A1. For more information, see “Base Address for Renesas RZ/A1 Flash Chip” in Appendix D, “Troubleshooting and Usage Notes” in *Green Hills Debug Probes User's Guide*.

Changes in Behavior

Changed Use of trace_clock_phase Value

The use of `trace_clock_phase` has been updated from previous releases. To calculate the new correct phase, use one of the following equations. If your old setting was greater than or equal to zero:

```
new_phase = old_phase - 127
```

otherwise:

```
new_phase = old_phase + 128
```

Changed Default of disable_swt Setting

The default for the **disable_swt** setting has changed from `off` to `on`.

Changes to Trace List Options

The **Disable trace when trace retrieved due to trigger** check box in the trace list options affects the **Retrieve trace when buffer fills** check box, because the **Retrieve trace when buffer fills** feature uses an internal trigger. If **Disable trace when trace retrieved due to trigger** is enabled, trace collection is disabled when the buffer fills up and trace is retrieved. Trace collection will not be automatically re-enabled for the duration of the connection.

To repeatedly fill and retrieve the buffer, disable the **Disable trace when retrieved due to trigger** option.

Defaults For jrst_ and rst_ Commands Changed

The following commands used to default to `300ms`, but now default to `10ms`:

- **jrst_pulse**
- **jrst_settle**
- **rst_pulse**
- **rst_settle**

New Probe Configuration Files

Some probe configuration files use the new **.ghpcfg** extension. They are similar to **.cfg** files, but are not yet supported in the graphical probe administrator (**gpadmin**). To load a configuration file with **mpadmin**, use the following command:

```
mpadmin -cfgload probe file.ghpcfg
```

MULTI 4 No Longer Supported

The 5.0.8 version of the probe support software no longer supports MULTI 4. If you attempt to install the software on MULTI 4, the 4.4.2 version of the probe firmware and support software will be installed instead.

Chapter 3

Version 4.4.4 Release Notes

Contents

This document covers changes to the Green Hills Probe firmware that were added for version 4.4.

New Features

New Supported Targets

- Intel Atom (Pineview) (`atom_pv`)
- Intel Atom (Tunnel Creek) (`atom_pv`)
- Intel Sandy Bridge (`sandy_bridge`)
- Freescale i.MX6 (`mx6`)
- Freescale Qorivva MPC560xE (`ppc560xE`)
- Freescale Qorivva MPC564xB (`ppc564xB`)
- Freescale Qorivva MPC564xC (`ppc564xC`)
- Freescale Qorivva MPC567xR (`ppc567xR`)
- Freescale Qorivva MPC5746M (`ppc5746M`)
- Freescale Qorivva MPC5744P (`ppc5744P`)
- Freescale QorIQ P3041 (`ppcP3041`)

Additional New Project Wizard Support

Unless otherwise noted, the following items require MULTI 5.2.4 or newer.

- Freescale Kinetis K70 (requires MULTI 6.1 or newer)
- Freescale MPC560x Demo Board (MPC560xE)
- Freescale MPC564x Demo Board (MPC564xB)
- Freescale MPC564x Demo Board (MPC564xC)
- Freescale MPC567x Demo Board (MPC567xR)
- Freescale MPC5746M Demo Board (MPC5746M) (requires Green Hills Compiler 2012.5.4 or newer)
- Freescale MPC5744P Demo Board (MPC5744P) (requires Green Hills Compiler 2012.5.4 or newer)

- Freescale P3041DS
- STMicro STM3240G-EVAL (STM32F407) (requires MULTI 6.1 or newer)

Support for Reading and Writing MPU Region Descriptors on Freescale MPC57xx

You can now use the **tlbr** and **tlbw** commands to read and write MPU region descriptors on Freescale MPC57xx targets. For example, to limit the first 64KB of SRAM so that it can only be executed in supervisor mode, use:

```
tlbw 0 0x40000000 Inst 0x4000ffff V,Sxsr,W
```

To make sure that it is set correctly, use:

```
tlbr 0
```

or, if you prefer to view all of the MPU entries in a table:

```
tlbr *
```

The probe's representation of the MPU index is as follows:

Probe	MPU
`0-5`	instruction-only entries `0-5`
`6-17`	data-only entries `0-11`
`18-23`	shared entries `0-5`

Support for Cortex-M4F VFP

This release adds support for the Cortex-M4F's VFP floating-point unit. To specify that your Cortex-M has a VFP, suffix the target type with `.vfp` when using the **set target** command.

Parallel Trace Decoding for ETMv3 Targets

This release adds support for ETMv3 parallel trace decoding, which increases trace processing performance for ETMv3 targets. This feature requires MULTI 6.1 or newer.

Chapter 4

Version 4.2.2 Release Notes

Contents

This document covers changes to the Green Hills Probe firmware that were added for version 4.2.

New Features

SWD Debug Interface Support

This release adds support for the SWD debug interface. For more information, see the documentation about the **use_swd** option in "ARM" in Chapter 4, "Probe Option Reference" in *Green Hills Debug Probes User's Guide*.

SuperTrace Probe v3 Debug and Trace Support for Additional Interfaces

The SuperTrace Probe v3 now supports debugging and tracing the following targets:

- ARM targets with ETM v3 and CoreSight debug interface
- PowerPC 55xx and 56xx targets with Nexus debug interface

For a list of supported targets, see "Supported Devices" in Appendix E, "Supported Devices and Adapter Types" in the *Green Hills Debug Probes User's Guide*.

BE8 Support for ARM11 and Cortex-R4

The probe now supports BE8 mode for ARM11, Cortex-R4, and the newly-added PJ4 and Cortex-A9 targets. For more information, see the documentation about the **be_mode** option in Chapter 4, "Probe Option Reference" in the *Green Hills Debug Probes User's Guide*.

New Supported Targets for v3 Probes

The Green Hills Probe and SuperTrace Probe v3 now support run control for the following targets:

- Cortex-A9 (`cortexa9`)
- OMAP 4 (`omap4`)

- ARM11MP (`arm11mp`)
- Marvell PJ4 (`pj4_v6`, `pj4_v7`)
- Cortex-M4 (`cortexm4`)
- Freescale Kinetis (`kinetis`)
- Cortex-M0 (`cortexm0`)
- PowerPC 564xA (`ppc564xA`)
- PowerPC 564xL (`ppc564xL_LSM`, `ppc564xL_DPM`)
- PowerPC 564xS (`ppc564xS`)
- PowerPC 567xK (`ppc567xK_LSM`, `ppc567xK_DPM`)
- PowerPC 440GR (`ppc440gr`)
- PowerPC 440EPx (`ppc440epx`)
- PowerPC 440GRx (`ppc440grx`)
- PowerPC 440SPe (`ppc440spe`)
- PowerPC 460GT (`ppc460gt`)
- PowerPC 460EX (`ppc460ex`)
- PowerPC 460GTx (`ppc460gtx`)
- PowerPC 460SX (`ppc460sx`)
- Applied Micro APM82181 (`apm82181`)
- PowerPC 405EX (`ppc405ex`)
- PowerPC 405EZ (`ppc405ez`)
- PowerPC 405EXr (`ppc405exr`)
- QorIQ P1020 (`ppcP1020`)
- QorIQ P1011 (`ppcP1011`)
- PowerPC MPC8308 (`ppc8308`)
- PowerPC MPC5125 (`ppc5125`)
- ColdFire 5441x (`cf54418`)
- Intel Atom (`atom`)
- Intel Core 2 (`core2`)
- Intel Nehalem (`nehalem`)

Note

The `atom` setting is for any Bonnell or Silverthorne device. Processors based on Pineview, Tunnel Creek, or later are not currently supported.

The `nehalem` setting is for any Core i3, i5, i7, or Xeon device based on the Nehalem architecture. Processors based on Sandy Bridge or later are not currently supported.

If you require support for a newer Atom, Core i3, i5, i7, or Xeon processor, contact Green Hills support.

For a list of supported targets, see “Supported Devices” in Appendix E, “Supported Devices and Adapter Types” in the *Green Hills Debug Probes User's Guide*.

Serial Port Forwarding Now Available

The Green Hills Probe and SuperTrace Probe v3 now support the **pterminal** command, which allows you to connect your target to your probe using the probe's serial port, and initiate a serial terminal session from your host machine over Ethernet.

Removed Features

Diagnostics Pane of Probe Administrator is Not Available in MULTI 6

The **Diagnostics** pane of the **Probe Administrator** will no longer be available after installing MULTI 6 or newer. This pane will continue to be available for MULTI 5.x.

New Online Probe Manuals No Longer Available for MULTI 4.x on Linux/Solaris

MULTI 4.x on Linux/Solaris uses a legacy help viewer that does not support newer manuals. If you have MULTI 4.x on Linux/Solaris, use the PDF documentation instead of the online help.

Chapter 5

Version 4.0.2 Release Notes

Contents

This document covers changes to the Green Hills Probe firmware that were added for version 4.0.2.

New Features

New Supported Targets for v3 Probes

The Green Hills Probe and SuperTrace Probe v3 now support run control for the following targets:

- QorIQ P4040 (`ppcP4040`)
- QorIQ P4080 (`ppcP4080`) — Revision 1.x silicon (`svr` = `0x82080010`) is not supported.

For more information about viewing registers on the P4080, see "Viewing QorIQ P4080 or MPC567xF Peripheral Registers in MULTI 5 Requires Configuration File Changes" on page 61.

For a list of supported targets, see "Supported Devices" in Appendix E, "Supported Devices and Adapter Types" in the *Green Hills Debug Probes User's Guide*.

SuperTrace Probe v3

Green Hills Probe firmware 4.0.2 adds support for the new SuperTrace Probe v3 hardware. This new model features:

- RoHS compliance
- A 4 GB or larger trace buffer
- External Trace Trigger I/O
- USB 2.0
- Gigabit Ethernet

For a list of supported targets, see "Supported Devices" in Appendix E, "Supported Devices and Adapter Types" in the *Green Hills Debug Probes User's Guide*.

selftest Command

The new **selftest** command runs several diagnostic tests on the probe's trace components. It is available on the SuperTrace Probe v3. For more information, see the Green Hills Debug Probes User's Guide.

Changes to Existing Features

Changes to Timestamps

The SuperTrace Probe v3 probe uses a new method to communicate timestamp data to **mpserv**. To collect timestamp data in MULTI from one of these probes, you must update your MULTI installation using the probe installer that ships with this release.

SuperTrace Probe v3 Does Not Have GPIO Pins

The SuperTrace Probe v3 does not have GPIO pins and does not support the **iop** command.

Chapter 6

Version 3.8.2 Release Notes

Contents

This document covers changes to the Green Hills Probe firmware that were added for version 3.8.2.

New Features

This section lists new features available in version 3.8.2.

Additional PowerPC Support

New PowerPC Processor Support

Supported Processor	Target String
PowerPC 8536	`ppc8536`
PowerPC 8569	`ppc8569`
PowerPC 560xB	`ppc560xB`
PowerPC 560xC	`ppc560xC`
PowerPC 560xP	`ppc560xP`
PowerPC 560xS	`ppc560xS`
PowerPC 563xM	`ppc563xM`
PowerPC 5668G/E	`ppc5668`
PowerPC 567xF	`ppc5674`
QorIQ P2020	`ppcP2020`

New PowerPC MULTI Project Wizard Entries

The following PowerPC boards are now available for stand-alone projects in the MULTI **Project Wizard**:

- Freescale MPC8536DS
- Freescale MPC8569-MDS-PB
- Freescale P2020DS

Entries for newly-supported PowerPC 56xx cores will be available in a future release.

TraceEverywhere Cabling System

New probe shipments for some architectures contain TraceEverywhere cabling, designed to provide longer cables with better reliability than the legacy cabling system. Over time, all architectures will be supported over a TraceEverywhere connection.

Changes and Fixes to Existing Features

This section lists changes and fixes to existing features in version 3.8.2.

Updated USB Driver

The 3.8.2 firmware ships with an updated version of the probe USB driver that supports additional operating systems, is easier to install, and is more reliable. This driver supports the following operating systems:

- Windows XP (32-bit)
- Windows Vista (32- and 64-bit)
- Windows 7 (32- and 64-bit)

This new driver is not backwards compatible with earlier versions of some probe software components. These components are updated when you perform a standard install from the probe CD that contains this firmware release.

If you are using Windows 2000, the installer installs the older version of the USB driver.

Probe Now Polls for Adapter and Power Status

If you have configured the probe to detect your target adapter automatically using `set adapter auto`, the probe now updates the setting whenever you plug in or unplug an adapter. It is no longer necessary to type `set adapter auto` or cycle the probe's outputs in order to refresh this setting. Removing an adapter now causes the probe to report an error. The probe also polls to check for the target's power status. The **checker** setting does not affect either of these polling behaviors.

Deprecated and Removed Features

This section lists features that have been deprecated or removed and are no longer supported as of version 3.8.2.

IDT32 Processors Are No Longer Supported

The IDT 32334, IDT 32335, and IDT 32438 processors are no longer supported. The last firmware to support these processors was version 1.4.1.

Chapter 7

Version 3.6.4 Release Notes

Contents

This document covers changes to the Green Hills Probe firmware that were added for version 3.6.4.

New Features

This section lists new features available in version 3.6.4.

New ARM Features

Support for New ARM Processors

The following ARM processors are now supported:

Supported Processor	Target String
ARM Cortex-A8	`cortexa8`
ARM Cortex-M3	`cortexm3`
Freescale i.MX51 Revision T02	`imx51_t02`
TI OMAP3	`icepick(3:omap3)`
TI OMAP2430	`omap2430`

In addition to supporting these new processors, this release improves support for ARM11, ARM920, and PXA320 processors.

New MULTI Project Wizard ARM Board Entries

The following ARM boards are now available for stand-alone projects in the MULTI **Project Wizard**:

Board Name	Notes
ARM Evaluation Baseboard Cortex-M3	
Freescale i.MX51 Boards (Babbage and Elvis)	
Logic PD OMAP 3430 Zoom SDK	
TI OMAP 3430 EVM	
TI BeagleBoard OMAP 3530	

Board Name	Notes
ST STM32F10x Evaluation Board	Full stand-alone MULTI flash support

Changes and Fixes to Existing Features

This section lists changes and fixes to existing features in version 3.6.4.

General Changed Features

Additional Commands Supported by gpadmin and mpserv

The **support** and **xswitch** commands are now available in the **Graphical Probe Administrator** (**gpadmin**) and **mpserv**.

Chapter 8

Version 3.4.1 Release Notes

Contents

New Features

This section lists new features available in version 3.4.1.

General New Features

New Probe Commands

The following commands are now available:

Command	Use
support	Prints information useful for Green Hills Support.
xswitch	Sets or modifies internal xswitches. Do not use this command unless instructed to do so by Green Hills Support.

For more information about these commands, see Chapter 5, “Probe Command Reference” in the *Green Hills Debug Probes User's Guide*.

New ColdFire Features

Support for New ColdFire Processors

The following ColdFire processors are now supported:

Supported Processor	Target String
MCF537x family (5372, 5372L, 53721, 5373 and 5373L)	`cf5373`
MCF5222x family (52221, 52223)	`cf52223`
MCF5225x family (52252, 52254, 52255, 52256, 52258, 52259)	`cf52259`
MCF5227x family (52274, 52277)	`cf52277`
MCF5445x family (54450, 54451, 54452, 54453, 54454, 54455)	`cf54455`

New MULTI Project Wizard ColdFire Board Entries

The following ColdFire boards are now available for stand-alone projects in the MULTI **Project Wizard**:

Board Name	Notes
Freescale ColdFire M5373EVB	
Freescale ColdFire M52223EVB	
Freescale ColdFire M52259EVB	
Freescale ColdFire M52277EVB	
Freescale ColdFire M54455EVB	See **board_info.txt** in your target resources project

New PowerPC Features

Support for New PowerPC Processors

The following PowerPC processors are now supported:

Supported Processor	Target String
PowerPC 8610	`ppc8610`
PowerPC 8641	`ppc8641`
PowerPC 8641D	`ppc8641D`

New MULTI Project Wizard PowerPC Board Entries

The following PowerPC boards are now available for stand-alone projects in the MULTI **Project Wizard**:

Board Name	Notes
Freescale HPCD 8610	Also known as Lyra
Freescale HPCnet (8641)	Also known as ArgoNavis

New sync_cores Option for PowerPC 8641D

The **sync_cores** option is now available for PowerPC 8641D targets. This option allows you to enable synchronous debugging, for use when debugging a program that shares memory between two cores. For more information, see the documentation for this option in the *Green Hills Debug Probes User's Guide*.

Changes and Fixes to Existing Features

This section lists changes and fixes to existing features in version 3.4.1.

General Changed Features

Changes to rst_tap_then_sys

Previous Green Hills Probe firmware releases included an option called **rst_tap_then_sys**, which controlled the waveforms generated on the JTAG TAP and CPU reset lines when the target was reset through the probe. This option has been enhanced, and renamed to **target_reset_pin**. If you set this option on your probe, consult the following table to determine which value to use for **target_reset_pin**.

rst_tap_then_sys Setting	Corresponding target_reset_pin Setting
`off`	`independent`
`on`	`freezes_tap` or `resets_tap`

For more information, see "Setting Reset Pin and JTAG TAP Interaction" in Chapter 4, "Probe Option Reference" in the *Green Hills Debug Probes User's Guide*.

ColdFire Changed Features

Improvements to the Detect Command

The **detect** command now detects all supported ColdFire processors, except for `cf5206e` and `cf5307`. If you are using one of these processors, set your target string manually.

MIPS Changed Features

EJTAG 2.5 Adapter Power Detection Fixed

The EJTAG 2.5 adapters have been modified to stop reporting erroneous power detection when the adapters were not plugged into a target.

EJTAG 2.5 Targets Ignore rst_pulse and rst_settle

For EJTAG 2.5 targets, the Green Hills Probe now implements a reset handshaking sequence with the target. Consequently, the **rst_pulse** and **rst_settle** times are ignored. Subsequent releases will give the option of either method.

Detecting External Reset on EJTAG 2.5 Targets

For EJTAG 2.5 targets, the Green Hills Probe now detects when an external (to the probe) reset has occurred by monitoring the `ROCC` bit of the `ECR` debug register.

Changes to the rr * Command

For MIPS32 and MIPS64 cores, the registers displayed using the **rr *** command are now limited to those that are available on target variant under test.

PowerPC Changed Features

Probe No Longer Sets MSR[SPE] After Target Reset

For PowerPC 55xx targets, the probe no longer sets the `MSR[SPE]` bit after target reset. If your application requires this bit to be set, you may set it in your setup script or in the appropriate target initialization code.

eTPU Is Available for Debugging

For PowerPC 55xx processors that have an eTPU, the probe now makes the eTPU available for debug as an additional core. For example, if debugging an MPC5553, the 5553 will be core 0, and its eTPU will be available as core 1.

MSR[SPE] Bit Not Set During Reset Sequence

Firmware previous to version 3.0.0 supporting MPC85xx processors set the `MSR[SPE]` bit as part of the reset sequence. In firmware 3.0.0 and higher, that no longer happens, and the `MSR[SPE]` bit remains 0 at reset. If your application requires the `MSR[SPE]` bit to be set, you may have to set it in your setup script, or set it in your initialization code, for proper operation. Also note that the probe's **vc** diagnostic tests require the `MSR[SPE]` bit to be set and will not pass otherwise.

Chapter 9

Known Issues and Limitations

Contents

This chapter lists known issues and limitations with the current probe release.

General Known Issues

USB Driver Installation Fails on Windows Vista

If USB driver installation fails on Windows Vista and you see a dialog box with the following message:

```
Windows encountered a problem installing the driver software for your device
```

1. Reboot your computer.
2. Run ***install_directory*/driver/drivertool.exe**.
3. Click **Install Driver**.

The second installation should work without any errors.

Cannot Downgrade Firmware On Some Probes

Due to a manufacturing change, probes with serial numbers 15000 - 15299 and probes with serial numbers greater than 15500 require firmware 3.6.4 or higher. The firmware on these probes cannot be downgraded to an earlier version.

MULTI 4/5 gpatch Does Not Roll Back On Linux/Solaris

On Linux/Solaris with MULTI 4 or 5, **gpatch** installing an update provides a new version of **gpatch** and uninstalling does not return **gpatch** to its original version.

Installation on MULTI 4 Clears Licenses

Installing the Green Hills Probe CD over a MULTI 4 installation will overwrite the **mpserv.exe** (Windows) or **mpserv** (Linux and Solaris) executable. Because licenses in MULTI 4 are stored in the executable, you must re-install licenses after installing the Green Hills Probe CD over a previously licensed MULTI 4 installation.

Installation Disables ecomarm2 License

If, after installing your probe software, **ecomarm2.exe** cannot obtain a license:

1. Navigate to your MULTI install directory.
2. Rename **ecomarm.exe** to **ecomarm.old**.
3. Rename **ecomarm2.exe** to **ecomarm.exe**.
4. Run `update.exe -i -f filename.lck -na ecomarm`.
5. Rename **ecomarm.exe** back to **ecomarm2.exe**.
6. Rename **ecomarm.old** back to **ecomarm.exe**.

Connecting to Multiple USB Probes via the Probe Administrator

On a system that has more than one Green Hills Probe or SuperTrace Probe connected via USB, it is not possible to specify which one to connect to via the **Add New Probe** menu option in the Probe Administrator. The first one will always be chosen.

To connect to additional probes connected via USB, run the Probe Administrator from the command line:

```
gpadmin -usb index
```

where *index* is the numerical index of the probe you want to connect to, beginning with 1.

Setup Script Fails when Running Diagnostics in the Probe Administrator

If you run diagnostics using the **diagnostics** pane in the Graphical Probe Administrator while your target is running, your setup script may fail. To work around this problem, halt the target before running diagnostics.

Issues Interleaving MULTI Script and mpserv Commands

In certain situations, if you issue a run-control command to **mpserv** after a MULTI run-control command, MULTI may not report the correct status of your target. This may cause a subsequent command to fail.

For example, if you issue the following commands in a board setup (**.mbs**) script or the MULTI Debugger's **cmd** pane:

```
>halt
>target run
```

and then hit a breakpoint, `target tc` may not cause the target to run, even in cases where the probe reports the target as halted. To work around this scenario, do not interleave MULTI script commands with debug server run-control commands. This issue is under investigation and will be addressed in a future release.

target tc and target th Behavior Changes when Halt Cores Synchronously is Selected

When the **Halt Cores Synchronously** mpserv connection option is selected, the behavior of the **target tc** and **target th** commands changes.

- **target tc** changes a core's status from `Stopped` to `Paused`. If all other cores are `Paused`, MULTI runs all cores.
- Similarly, **target th** changes a core's status to `Stopped`. If any other cores were running, MULTI changes their status to `Paused`.

You may need to modify your setup script if it contains **target tc** or **target th** commands that are directed to specific cores via the **t** command (e.g., `target t 3..4 th`). Instead of using **target tc** or **target th**, use `groupaction -r @all` to resume all cores and `groupaction -h @all` to halt all cores.

Break on Trigger Only Halts Target If Target is Not Already Halted

If you use the target-specific **Break on Trigger** trace option, the probe does not halt the target if the target is already halted when the trigger is hit. On ETM targets, if you have enabled this setting, have an execute trigger set on an address range, and are halted in that range, the trigger occurs immediately; the probe does not halt the target after you run.

Missing Documentation for Exceptions in the Set Triggers Window

The documentation for the **Set Triggers** window is missing information for a few items:

- The **Exception** option makes the trigger active when the specified exception is taken. It is only available on ARM ETM targets.
- The exception type descriptions that end in **(High)** are intended for applications that use high exception vectors (starting at `0xffff0000`).

Setting Options in the Trace Options Window Has No Effect When Data Trace is Disabled

When **Data Trace** is not enabled in the **Trace Triggers** window, MULTI will still allow you to select different **Data Capture** modes in the **Trace Options** window, but trace data will not be collected.

Slow Trace Decompression on Windows While the PathAnalyzer or Trace List is Open

On Windows hosts running MULTI 5 or earlier, trace data is decompressed very slowly while the **PathAnalyzer** or **Trace List** is open. While you can use these windows to control trace, start trace retrieval, or check on the decompression process, if your trace buffer is large (> 100 MB) you should close them when they are not in use. You can reopen the windows after the decompression process is complete.

Gap Between Timestamps in the Trace List or Path Analyzer

When the host buffer is full, MULTI attempts to discard unnecessary trace data. This behavior may cause side effects as buffers are discarded over time, such as a gap when viewing timestamps in the **PathAnalyzer** or **Trace List**.

Trace Data Lost when Trace is Disabled Immediately After Retrieval

When controlling trace operations through a MULTI script, trace data collected while the target was running may be lost due to a race condition when trace is turned off, trace data retrieved, trace is turned on, and the target is run.

Because it is a race condition, this issue only occurs when these commands are run consecutively in a setup script; it does not occur when you execute these commands manually. To work around this issue, insert a `wait -time 1000` command between trace retrieval and turning trace on.

AddressSpaces Not Traced by Default After Disabling Trace

When you right-click any AddressSpace in the Debugger's target list and clear the **Trace** menu item, subsequently created AddressSpaces are not traced by default. To work around this issue, manually activate trace for new AddressSpaces.

TimeMachine Demo Requires Specific Trace Options

In order to run the TimeMachine demo, you must select the following options in the **Trace Options** window:

- **Automatically enable trace collection**
- **Retrieve trace when target halts**
- **Retrieve trace when buffer fills**

Some Tabs are Empty in the Register View Window

Some peripherals are not initialized by the default setup script. If you attempt to access an uninitialized peripheral, you can put the target in a bad state. For this reason, registers that are not initialized are sometimes marked *hidden* in the register definition (**.grd**) file, and do not display in the **Register View** window. In some cases, an entire group of registers is hidden, so the tab for that group in the **Register View** window is empty. To view these registers, make the following modifications to your **.grd** file:

1. Look for registers with the attribute `hide = ${`*`FLAG`*`}`
2. Change the value of *FLAG* to `false` to show all registers marked with that flag.

Tracing a Program Running from ROM with a Setup Script

When running out of ROM while using a setup script and trace enabled, the probe will trace the action of the setup script, which may result in decompression errors. To resolve this, issue **trace clear** after running the **setup** command. You can also add **trace clear** to the end of your setup script.

TE Pod logic_high Setting

TE Pods through Revision D (serial numbers less than 1000) cannot reliably drive the following pins of the following adapters when the setting for `logic_high` is greater than 3.5 volts. These pins will still continue to function as inputs.

- MIPI-34 — `DBGACK` and `nTRST_PD`
- MIPI-60 — `TRIGOUT` and `TRST_PD`
- Nexus-HS22 — `EVTI`
- Nexus-HS34 — `GEN_IO3` and `GEN_IO5`
- Nexus-HS70 — `EVTI`
- Nexus-HP50 — `BOOTCFG` and `TOOLIO5`
- Nexus-MICTOR — `BOOTCFG`
- MIPS-PDTrace-MICTOR — `TR_TRIGOUT` and `TR_PROBE_N`
- TI14 — `EMU0`

If `logic_high` is set above 3.5V any affected pins will automatically be tri-stated. If any of these pins need to be driven, set `logic_high` to 3.5V or lower. Most targets that use a `logic_high` above 3.5V will work properly with a `logic_high` setting of 3.5V. You must reboot your probe or reconnect your adapter if you change `logic_high` within the supported range after a pin had been tri-stated.

Enabling Outputs Does Not Report an Error with Incorrect TE Adapter Setting

When the `adapter` setting is not set to `auto` and you connect a TE Adapter, the probe's outputs will be tri-stated and cannot be reenabled until the `adapter` setting is changed to `auto`. Neither of the two methods of enabling outputs (**jp on** command,

or pressing the **user** button when `user_button` configuration option is set to tri-state) will reflect this error, and it will appear to succeed even though outputs remain tri-stated.

Issues Updating Probe Firmware

If you encounter an error updating firmware on your probe:

1. Try updating again.
2. Reboot the probe and try updating the firmware again.
3. If the same error persists, contact Green Hills Support.

This is most likely to occur with probes that have serial numbers between 10001 and 10120, and may also happen with probes that are being updated from a firmware version earlier than 5.0.2.

RTCK Failure Can Cause Long Delays

If `use_rtck` is enabled and your target's RTCK pin stops working (due to a target problem, power failure, or similar), then the probe may become unresponsive for long periods of time. If this happens, restore your target to a known working state and either wait for the probe to recover or power cycle the probe.

ARM Known Issues

Cannot View I-Cache or L2 Cache on Cortex-A5 Targets

For Cortex-A5 targets, the MULTI **Cacheview** window allows you to select `I-cache` and `L2 cache`, but no data is available or will be displayed for these caches.

Cannot Debug Certain Cache Configurations on Cortex-A5 and Cortex-A9 Targets

The probe is unable to step off breakpoints on Cortex-A5 and Cortex-A9 targets when the L1 I-cache is enabled, L1 D-cache is disabled and the L2 cache is enabled. If the L1 D-cache is disabled, then the L2 cache must also be disabled or debug features including (but not limited to) software breakpoints may be disabled or unreliable.

Many TMS570 and R4x Processors Incorrectly Detected as a Cortex-R4F

Many TMS570 and R4x boards are incorrectly detected as a Cortex-R4F. If you have one of these targets connected to the probe, run the following commands to configure the probe correctly:

```
> dlh
> detect
> set target icepick(0:cortexr4)
```

No Access to XScale Cache Operations Register

The probe does not implement access to XScale coprocessor 15 register 7 (the cache operations register), but when it writes to the target's memory, it flushes the I-cache lines and cleans the D-cache lines to which the memory write maps. It also flushes the write buffer before resuming the target. That said, the lack of explicit cache invalidate, clean, and allocate commands may make it difficult to set up a bare board. Contact Green Hills support for information about when these facilities will be implemented.

bl Displays Duplicate Breakpoints

Under certain conditions, the **bl** command displays duplicate entries for breakpoints. These duplicates do not indicate a problem, and can be ignored.

Slow Halt On ARM920 Target

Halting an ARM920 with a slow JTAG clock and caches enabled may take a long time. This problem is most frequent with an AT91RM9200 running an application in ROM. To increase speed, configure the probe with the following command:

```
xswitch -tmpl_arm7_arm9.upload_arm920_dcache_on_halt
```

When using this setting, **Cacheview** does not work.

Trigger Immediately Causes Two Triggers on CoreSight ETM11 Target

Due to a workaround for ARM erratum 350999 that affects CoreSight ETM11, using **Trigger Immediately** on an ETMv3.2 target may result in two triggers.

Cannot Collect Trace Data on a Trigger on OMAP3

Because the TI OMAP3 does not connect the ETM trigger to the TPIU trigger output, the SuperTrace Probe cannot collect data on a trigger on this target.

Freescale i.MX51 Does Not Work at Slow Clock Speeds

The Freescale i.MX51 may not work reliably with `TCK` speeds slower than 8 kHz. It does work reliably at higher speeds. To work around this issue, use a higher clock speed.

Trace Count For Accesses To or Execution Of a Single Address on ETM Targets

For ETM trace, if you are counting accesses to or execution of a single address with a count, the count is exact. It counts the number of times the address was accessed or executed. If you are counting accesses to or execution within an address range

or a symbol the count is sticky. It counts the number of cycles between access or execution of an address in the range and access or execution of an address outside the range. For practical purposes, this means that using a count with an address range is unlikely to yield the desired results.

Trace May Not Decode Correctly While Booting Cortex-A INTEGRITY Systems

If the trace system is enabled while a Cortex-A INTEGRITY system is booting by download, it will collect trace data of boot loader execution and secondary core spin loops in the boot MMU configuration, which may not match the MMU mappings used after the kernel is up and running. If this happens, the affected portion of the trace buffer will not decode correctly and may abort and/or cause errant memory reads from the target if the corresponding trace decode options are enabled.

To work around this issue, disable trace until after secondary cores are booted during BSP initialization. An alternative workaround is to disable decoding abort on opcode failure and reading unknown opcodes from the target, and disregard the incorrect portion of the trace buffer which occurs before secondary core initialization.

Missed Trace Triggers in INTEGRITY Virtual AddressSpaces

On the AT91RM9200, a trace trigger may be missed if trace is disabled in an INTEGRITY virtual AddressSpace while the trigger condition is met in that AddressSpace. To work around this issue, re-apply trigger settings or re-enable trace after modifying which address spaces are traced.

Some ARM Cores Must Be Halted When Enabling Trace

Some ARM cores, such as the ARM1156, ARM1176, and PJ-4, must be halted when trace is enabled. If you are using one of these cores, either:

- Enable trace manually, only when the core is halted, or
- pass the **-Xetm_halt_to_trace** argument to **mpserv**. This command halts and then resumes the target as needed when enabling trace.

ARM ETM 64-Bit Data Accesses Displayed as 32-Bit Accesses in Trace List

When tracing ARM ETM targets, the **Trace List** displays 64-bit data accesses as two 32-bit accesses.

In MULTI 5, Trace Does Not Work in BE8 Mode for Some ARM Cores

Tracing an ARM11 or Cortex-R4 target in BE8 mode on MULTI 5 is not supported. If you need to trace one of these targets in BE8 mode, use MULTI 6 or newer.

Probe Cannot Detect Some ICEPick Targets

If your target has an ICEPick, and there is a device on the JTAG scan chain that is not controlled by the ICEPick, the probe's **detect** command will not be able to detect your target.

Some Data Missing from Trace Buffer on Cortex-M3 Targets

Some Cortex-M3 targets do not properly flush all trace to the SuperTrace Probe when halting. Due to this issue, small amounts of data from the end of the trace buffer may not be captured. To reduce the frequency of this issue, use a larger port size.

Some ARM11 CPUs Cause Incorrect Trace Data

Some ARM11 CPUs, including the Freescale i.MX31, contain a hardware erratum that can cause trace errors and incorrect trace when tracing execution in Virtual AddressSpaces. For more information, see ARM erratum 351599.

Break on Trigger Does Not Trace Final Instruction on Cortex-R4

When the **Break on Trigger** check box is enabled, some Cortex-R4 targets do not trace the final instruction before halting due to a trigger.

Enabling Trace on Multiple Running Cores

Multi-core trace on ARM targets is enabled on each core sequentially. This means that if one or more cores are running when trace is enabled, you will capture a small amount of trace of the first enabled core before capturing any trace from the next one, and so on. If you are using a small trace capture buffer (such as ETB) and retrieving trace when the buffer fills or due to a trigger, you may fill your buffer or hit your trigger condition prior to trace being enabled on all cores. This can result in no trace being captured for some cores. One workaround is to halt cores you want to trace prior to enabling trace. Another is to choose your triggers with this behavior in mind, or manually enable/disable trace.

ARM Multi-Core Trace Targets with MULTI 6.x and Earlier May Require Enabling Trace Manually

Multi-core trace on ARM targets requires access to trace registers on each core when trace is initialized after the setup script is run. If your setup script does not enable access to those registers on all cores, trace will not be automatically enabled on those cores, and you may see the error message `Debug server failed to connect to TraceServ`. When the trace registers are available, you can manually initialize trace on those cores by taking a trace action (such as opening a trace window like the **Trace List** or **Trace Options** window).

At that time, if the check box **Automatically enable trace collection** is selected, trace will be initialized again, which may cause problems if you are currently collecting or retrieving trace on another core. We recommend clearing that check box and manually enabling trace. When manually enabling trace, first download to all cores, initialize trace on all cores, and then enable trace.

Tracing ARM Targets Triggering Close to the Beginning of the Trace Buffer

ETM and PTM trace (all versions) output a periodic synchronization sequence, generally every 1024 bytes of trace. When decompressing trace, everything prior to the first synchronization sequence is discarded. If your trace buffer size and trigger position are configured so the trigger might be in the first 1024 bytes of the buffer, trace will still trigger and collect, however there may be no indication of the trigger position in the decompressed trace if it was discarded prior to the first synchronization sequence.

Function and Callees Filter Issue

On a Cortex-A9, if you create a trace filter using **Trace on: Function and Callees Executing**, the first instructions of the specified function (up to and including the first branch) might not be traced.

SWD May be Unreliable on Freescale Vybrid

The Green Hills Probe cannot reliably debug a Freescale Vybrid using SWD. To work around this issue, use JTAG to debug Freescale Vybrid SoCs. For more information, see "Selecting the Target Communication Protocol" in Chapter 4, "Probe Option Reference" in *Green Hills Debug Probes User's Guide*, or contact Green Hills Support.

Flash Programming May Be Unreliable on Renesas RZ/A1 Board

Writing to flash on the Renesas RZ/A1 board may be unreliable with gflash. If a write failure occurs, erase the flash, and try the write again. The second write will usually work, but in the rare case that it also fails, a third attempt will succeed.

Data Trace of Load/Store Multiple Instructions on ARM Targets with ETMv3.x with Incomplete Data

In some cases, a Load/Store Multiple instruction will not output trace packets for all data transactions that occurred. In this case, TimeMachine will treat the data transactions that were output as the last transactions. For example, if you trace an LDM instruction that loads data into registers R3, R4, and R5, but there are only two traced data transactions, those data transactions will be traced as having been loaded into R4 and R5. This behavior is as specified in the ETMv3 specification, but there are cases where hardware does not behave according to the specification that can result in incorrect TimeMachine memory and register reconstruction.

If you encounter a case where a Load/Store Multiple instruction is traced, some but not all of the data transactions are traced, and the reconstructed values appear to be incorrect, please contact support.

ColdFire Known Issues

Power Detection Limitations

Power detection is not supported for the 5235, 5271, and 5275. When using these processors, turn off power detection with the following probe command:

```
set power_detect off
```

Breakpoint Limitations

Breakpoints on virtual tasks or virtual memory areas are not supported.

Detecting a ColdFire Target with SuperTrace Probe

To detect a ColdFire target with a SuperTrace Probe, the target should first be set to a ColdFire target before issuing the **detect** command. For example, the following sequence will work reliably:

```
jp off  set target cf5249  detect
```

If the target is not set to a ColdFire, the SuperTrace Probe will attempt JTAG detection, which does not work with ColdFire targets. The Green Hills Probe does not have this limitation.

MIPS Known Issues

freeze_timers Disables the EN Bit in CTC1, CTC2, and CTC3

For IDT32438 targets, the **freeze_timers** option will freeze the core's general-purpose 32-bit counter/timers by disabling the `EN` bit in `CTC0`, `CTC1`, and `CTC2` while the target is in debug mode. When this option is enabled, any attempts to access these memory-mapped registers will not give the desired result. If you want to write to them, you must ensure that the **freeze_timers** option is off when the target is halted right before accessing these registers, or off when the target is run right after accessing these registers.

Low Level JTAG Procedures May Disrupt M4K Processors

When debugging an M4K processor, some low level JTAG procedures may disrupt the processor for a short time, causing problems with run control. The **detect** command is an example. This issue is being investigated, and should not cause problems during normal debugging.

Stepping Off of Breakpoints May Not Work When Debugging a Virtual Task

When debugging a virtual task (for example, using OSA), stepping off of a breakpoint may not work. If you encounter this problem, launch **mpserv** with the **-X_virtualPPC** argument.

Hardware Breakpoint Types on the Au1500

The Au1500 allows for two kinds of hardware breakpoints:

- *Watchpoint style* — These cannot match data, and the 3 least significant bits of the mask must be 0. (This means you cannot set a breakpoint on a single instruction, or single `int`.)
- *EJTAG 2.0 style* — (not supported by Green Hills Debug Probes) These only look at the system bus, so they cannot differentiate between instruction/data loads, and do not work well when running from cached memory. If you require

the capabilities of the EJTAG 2.0 style hardware breakpoints, contact Green Hills Software.

Accessible Physical Address Range Limited to 512 MB

The Green Hills Probe accesses physical memory on MIPS through a 512 MB window at `0xa0000000` or `0xfffffffffa0000000`. This corresponds to a physical address range between `0x00000000` and `0x1fffffff`. Accesses outside the range fail, causing the probe to print the following error to the console:

```
ERROR 55 (memory read error): Memory read failed ERROR 14 (invalid parameter):
Currently physical addresses greater than 0x20000000 are not supported.
```

If you are debugging a kernel that references addresses outside this range, OSA support in the MULTI Debugger may also be limited.

This issue affects all firmware revisions from 3.0.0 to the current release.

TC Restrictions on MIPS 34K and 1004K Processors

The setup script activates only the first TC of each core on MIPS 34K and 1004K processors. Also, **mpserv** will not allow programs to be downloaded to RAM using alternate TCs. To work around this, use the first TC to download and run programs. The program running on the first TC should configure and activate alternate TCs.

Power Architecture Known Issues

Incorrect Trace Decoding on PPC405 Processors

If the first broadcast in a trace capture is one of the following, trace decoding may provide incorrect data:

- INTEGRITY TaskContext information branch
- `mtctr`
- `mtlr`
- `sync`

If you run into this issue, contact Green Hills Support.

MPC5744P Stalls With Certain Trace Settings

The MPC5744P may stall indefinitely when:

- **Stall Processor to Avoid Overflows** is set to `on`
- **Use Branch History Messages** is set to `off`
- **Trace Clock Multiplier** is set to `1/1x`

This issue is under investigation by Freescale. We recommend enabling branch history messages or using a `1/2x` trace clock multiplier when tracing this target.

Incorrect Trace With PowerPC e200 and MULTI 6

When tracing a PowerPC e200 target with MULTI 6, if you are using the **Trace on:** feature, the instructions shown for the beginning of trace after the `start` event may be incorrect. This may also result in trace errors. The instructions become correct again after a direct branch, or if branch history mode is enabled, after an indirect branch. This issue will be fixed in a future version of MULTI.

Censorship Unlock Requires Two Resets on PPC560x Processors

When using the probe's **censor_unlock** option to unlock a PPC560x target, the probe may need to reset the target twice in order for the unlock to succeed.

Viewing QorIQ P4080 or MPC567xF Peripheral Registers in MULTI 5 Requires Configuration File Changes

The probe software includes full peripheral register definitions for the QorIQ P4080 and MPC567xF, but, for performance reasons, they are hidden from **Register View** in MULTI 5 by default. To view a group of these registers:

1. Open ***install_dir*/defaults/registers/p4080_actual.grd** or ***install_dir*/defaults/registers/ppc_567xF.grd**.
2. After the comments at the top of the file, there are one or more register group definitions that disable each group. To enable a group, change the `0` next to the group's definition to a `1`.
3. From the **Register View** window, select **File → Reinitialize Register Information**. The newly-enabled registers should now appear.

For Green Hills Probe connections, you can improve performance by connecting to one core only. To specify which core to debug, use the **-force_coreid** option with **mpserv**.

Little Endian Mode Is Not Supported on PowerPC e500-, e500mc-, e5500-, or e6500-based Targets

Little endian mode is not currently supported on PowerPC e500-, e500mc-, e5500-, or e6500-based targets.

Incorrect PC Location After Halting Target

On PowerPC 603, 7xx, 5200, and 82xx, processors, if the processor is spinning at a branch-to-self opcode (`0x48000000`) that is in memory as the last instruction in an I-cache line (for example, at an address ending with `0x1c` or `0x3c`), and the I-cache is enabled, then halting the processor may result in a reported PC that is

four bytes past the true PC. This happens as a result of branch folding, and is currently being investigated with Freescale.

One of Freescale's recommended workarounds is to set a hardware breakpoint, which disables the branch-folding behavior. On PowerPC 7xx processors, the probe sets a hardware breakpoint as long as the **disable_swbp** option is set to `off`.

Locked Data Cache Not Supported on PowerPC 4xx Targets

The probe does not currently support locked data cache. It is possible to set up locked cache lines with no memory backing them, and this is fully supported by the hardware, but the probe does not properly handle this situation with the current firmware. This configuration will be supported in a future release.

Corrupted Registers When Setting an Execute Hardware Breakpoint on Some PowerPC Cores

Registers on PowerPC 8343, 8347, 8349, 8358, and 8360 cores may become corrupted if you set an execute hardware breakpoint that has a range which includes the next instruction to be executed.

Register Definitions Require Setting MULTI Variables

Version 3.8.2 of the probe firmware includes full register support for three PowerPC targets: P2020, MPC8536, and MPC8569. The addresses of all peripheral registers on these targets are offset relative to the CCSR base address. To enable MULTI to read these peripheral registers, you must define the CCSR base address using the following MULTI variables:

```
eval $E500_CCSRBAR_IS_SET=1
eval $E500_CCSRBAR= CCSR_base_address
```

We recommend adding these lines to an **.mbs** or **.rc** script that you use to debug your target. These lines are already present in the included **.mbs** scripts.

External Trace Trigger In Not Supported on PowerPC 405 Targets

External trace triggers sent to the probe's **Trigger In** port are not supported on PowerPC 405 targets at this time.

Modifying Trigger Settings on PowerPC 4xx Targets

Trigger settings on PowerPC 4xx targets cannot be modified unless the target is halted. If you modify these settings while the target is running, the change is deferred until you halt the target. If you enable trace while the target is running, triggering is not active until you halt and resume the target. No warning or error is issued.

MPC564xC z0 Core Does Not Emit Trace Data on Single Step

While the MPC564xC z0 core supports trace, it does not emit trace data when the target is stepped. If you perform an instruction step on a load or store, no trace data is collected for that instruction.

Trace Errors With Code That Switches Between VLE and Non-VLE Modes

In MULTI 5, when tracing code that switches between VLE and non-VLE mode on e200 processors, there may be errors in the trace listing shortly after a mode change. Specifically, the trace listing may show instructions in the wrong VLE mode. This is most likely to happen if one of the following occurs shortly after a VLE mode change:

- stalling is enabled and the CPU stalls to prevent a FIFO overflow
- the CPU hits a breakpoint
- the CPU executes 256 instructions with no branches
- branch history mode is enabled, and the CPU executes a total of 32 or more direct branches with no indirect branches in-between them

To minimize the chances of this type of error, we recommend tracing with the highest available MDO width and trace clock multiplier. Disabling data trace may help, and in some cases, disabling branch history mode may also help.

Nexus Trace Does Not Support Read- or Write-Only Triggers

Nexus trace supports read/write triggers that trigger on a read or write, but it does not support read-only triggers or write-only triggers.

Nexus e200 MDO Width Limitations

For e200 targets that support parallel Nexus trace, check your target documentation to determine supported MDO widths for your specific chip package. The probe supports tracing targets with 2-, 4-, 8-, 12-, and 16-bit MDO widths. 2- and 8-bit widths are only supported with MULTI 6 or newer. 16-bit widths are only supported with MULTI 6 or newer and the Nexus TraceEverywhere trace pod.

Nexus e200 Trace Is Only Supported on One Core at a Time

On Nexus e200 targets with more than one core, such as the MPC5516, MPC5668, and MPC5643 (in dual-processor mode), you can only trace one core at a time. By default, the probe traces core 0. To trace the second core, connect to **mpserv** using the **-nexus_trace_coreid 1** option and run your setup script on the core you want to trace. For example, if you have multiple executables to download to your target:

1. In the MULTI Debugger, select the core you want to trace.
2. Use the **load** command to run the script on the core.
3. Select each additional core and use the **load -nosetup** command to prepare it.

If you have a single executable:

1. In the MULTI Debugger, select the core you want to trace.
2. Use the **prepare_target -allcores** command to prepare all cores.

After all cores are prepared, resume the target to begin your debugging session.

Support for tracing both cores at the same time will be added in a future release.

Standard Nexus Trace Adapter Does Not Support 5 V signals

Tracing a 5 V target is not supported with the Nexus trace adapter. If you need to trace or debug one of these targets with a SuperTrace Probe V3, contact Green Hills support.

Single Stepping Over mtspr dbsrwr, rn May Not Execute As Expected on QorIQ P4040 and P4080

When the **edm** option is set to `off`, single-stepping over a `mtspr dbsrwr, rn` instruction may not execute as expected. The `dbsr` bits may not be updated. To work around this issue, avoid single-stepping over or setting breakpoints on `mtspr dbsrwr, rn` instructions.

Triggers Are Not Supported on the e200z0 Core of the MPC564xC

Triggers are not supported on the e200z0 core of the MPC564xC processor.

Incorrect Error Message When Tracing A 564xB or 564xC

If you use MULTI 6.1 and trace a 564xB or 564xC target with 8-bit MDO width and data trace enabled, the following error message may appear when a 1-byte data access occurs in the trace data:

```
Error: Invalid Data Packet. Trace data is corrupt.
```

This error can be ignored and does not affect the correctness of trace. This incorrect error message will be removed in a future probe release, and has already been removed in MULTI 6.1.4. This message does not occur when using 12-bit MDO.

Unexpected Machine Check On 567xR and 567xF

On 567xR and 567xF processors, if a target hits a software breakpoint within 7 non-branch instructions preceding an opcode that is expected to cause a machine check interrupt, the interrupt may occur even if, prior to resuming, the target state is changed so that the machine check condition is no longer met. To work around

this issue, place your software breakpoint at least 8 instructions before any opcodes expected to cause machine checks.

Trace Limitations with Stalling Enabled on MPC5777M e200z7 Cores

When the **Stall Processor to Avoid Overflows** trace option is enabled on an MPC5777M e200z7 core, trace data may be corrupted if trace is enabled or disabled while the core is running. Always halt an MPC5777M e200z7 core before enabling or disabling trace, or disable stalling.

Incorrect Trace Decoding on MPC5777M Processors

If branch history mode is disabled while tracing an e200z7 core of an MPC5777M processor, and the PC is changed while in debug mode, then one or more instructions in the trace list may be wrong after the target is resumed. This does not occur with branch history enabled, or with the e200z4 core. This issue is being investigated with Freescale.

Incorrect Trace Decoding on MPC577xK Processors

If branch history mode is disabled, and more than one core on an MPC577xK processor is being traced, there may be an occasional corrupt trace packet that results in trace errors. This does not occur with branch history enabled. This issue is being investigated with Freescale.

Example T4240QDS Setup Script Should Not Be Canceled

If using MULTI 6, do not cancel execution of the example T4240QDS setup script provided by the stand-alone New Project Wizard. Instead, wait for the script to run to completion.

Multi-Core Debug Limitations on QorIQ P3041

In rare cases, running certain multi-core applications on the QorIQ P3041 can cause the target to become unresponsive. When this happens, the probe lists the cores'

status as `unknown`. To recover from this state, reset the target. This issue is being investigated with Freescale.

Trace Errata on Certain P4080/P4040 Silicon Revisions

Early silicon revisions of the P4080 and P4040 contain errata that can cause significant corruption of trace data. Affected silicon is identified by a major revision value of `1` or `2` in the SVR register.

Examples of affected SVR values:

- P4080: `svr=0x82080010` or `svr=0x82080020`
- P4040: `svr=0x82090010` or `svr=0x82090020`

Use P4080/P4040 silicon with major revision `3` or greater to avoid this issue.

x86 Known Issues

x86 TraceEverywhere Adapters Not Supported with TraceEverywhere Trace Pod

The current hardware revisions of x86 TraceEverywhere adapters are not supported with the TraceEverywhere trace pod. An updated revision of these adapters will be available in the future.

Probe Cannot Configure Memory Mapping

The probe expects that your target already has a 32-bit flat memory mapping configured; it cannot create this mapping on its own. 16-bit code segments and segmented memory access are not currently supported.

We recommend that you use a boot loader to initialize your target. For example, a USB stick configured to boot GRUB could quickly boot and initialize your target. For additional information, see ***install_directory*/target/86/generic/board_info.txt**.

tr Command Does Not Work as Expected on Some x86 Targets

Certain x86 targets require 10-15 seconds to reset. If you are having difficulty when issuing the **tr** command to your target, try increasing the **rst_settle** setting.

MULTI Reports Any x86 Processor as a Pentium Pro

When connecting to your target with MULTI, MULTI reports the CPU as a Pentium Pro. MULTI does not have settings for newer processors at this time.

64-Bit Mode Debug Is Not Yet Supported

64-bit mode debug is not yet supported. This includes accessing registers specific to the 64-bit mode, as well as 64-bit memory addresses.

Access to MSRs or IO Memory Is Not Yet Supported

The probe does not provide access to MSRs or IO memory at this time.

Cannot Write to Segment or Table Registers

The segment registers and table registers are currently read-only.

Simultaneous Run-Mode and Freeze-Mode INTEGRITY Debugging Is Not Supported

Simultaneous debug of INTEGRITY via run-mode (**rtserv**) and freeze-mode (**mpserv**) is not supported at this time. Use the **enable_debug** setting to specify whether the probe or the target handles debug exceptions.

You can set freeze-mode software breakpoints on Sandy Bridge targets without having any effect on run-mode debugging. Doing so still requires an appropriate setting for the **enable_debug** option.

INTEGRITY run-mode partnering is not currently supported on x86 targets.

Halt and Breakpoints on Sandy Bridge Targets Is Synchronous

The halt feature and breakpoints on Sandy Bridge are synchronous. When halting or breaking on any one core using the probe, all cores on the target halt, including cores that are not configured in the JTAG scan chain. It is not possible to halt one Sandy Bridge core and leave other cores running. The resume feature is not a synchronous operation by default. Halting a core halts all cores, but resuming that core may not resume the other cores. Synchronous resume is possible using the MULTI **groupaction** command, or the probe's **gc** command.

Running Programs that Change Address Mappings

To download and run a program that changes address mappings (such as an INTEGRITY kernel) on an x86 target, use the **-load_physical** option when connecting to your target. When using this option, you will not be able to set software breakpoints in your code until the address translation mapping is enabled, but

hardware breakpoints will work. To work around this issue, set a hardware breakpoint that resets all software breakpoints shortly after the kernel starts running.

For example, if you are using INTEGRITY, you can set a hardware breakpoint by adding the following lines to your **.mbs** or **.rc** setup script:

```
configure continuePlaybackFileOnError on
hardbrk execute __ghs_ind_crt0 { Tog q off ; Tog q on ; resume }
configure continuePlaybackFileOnError off
```

This hardware breakpoint allows you to set software breakpoints before downloading your program. You can manually remove it during your debugging session if you need to use the hardware breakpoint slot that it occupies. If you do not remove the breakpoint and you run the program multiple times without reloading it, MULTI will warn you that this breakpoint is already set. You can ignore this warning.

If you need MULTI to handle system calls, use the **-hwbpsc** option when connecting to your target to use a hardware breakpoint to catch system calls.

Target Strings for Multi-Core and SMP Debugging

To debug both cores of a Core 2 processor, add the suffix `.duo` to the target string. For example, if your board has two Core 2 processors (and no other devices on the JTAG scan chain) and you want to debug all four cores:

```
> set target core2.duo core2.duo
```

If your target has an Atom- or Nehalem-based processor and you want to access both threads, add the suffix `.ht` to the target string. For example:

```
> set target atom.ht
```

Software breakpoints are not currently supported in an SMP environment.

Threads that are bound to the same core are always either both running, or both halted. They cannot be run or halted individually. If one thread hits a breakpoint, both threads halt. Stepping a thread may also be unreliable.

Booting a Multi-Core Target After Reset

Targets with Intel x86 processors typically have a BIOS check that prevents them from completing their boot sequence unless all cores are running. Be sure to resume all cores after a reset to allow for the BIOS to complete its startup sequence.

Booting a Multi-Core OS Clears Hardware Breakpoints on Secondary Cores

When any core is reset on an x86 target, hardware breakpoints set on that core are cleared. After the core begins to boot, you can halt it and set hardware breakpoints. Because booting a multi-core OS (such as INTEGRITY) on an SMP system causes secondary cores to go through a reset sequence, you should set hardware breakpoints on these cores after booting the OS.

Target Halts in System Management Mode Code

Some x86 targets enable system management mode (SMM). If SMM is enabled and you halt the target, it may halt in SMM code. If you did not intend to debug SMM code, resume the target and try halting again.

When SMM is enabled, the **vc** and **vrh** diagnostics may fail.

Nehalem-Based Target Cannot Leave System Management Mode

Some Nehalem-based targets have a BIOS that performs a processor coherency check while in system management mode (SMM). This check asserts if any of the processors are not running. This may happen while debugging the system via JTAG if one core is halted while the others run. One of the running cores may assert, which causes the system to remain in SMM until restart. In this case, you may see a printed assertion in **SmmDispatcher.c**. To avoid this assert, halt and resume all cores simultaneously using the group run and group halt commands (see the documentation about synchronous run control in the *MULTI: Debugging* book). On such systems, software breakpoints and hardware breakpoints will probably not work, because they only halt one core. Synchronous breakpoints will be supported in a future firmware version.